Subsequent is an annealing process at a temperature in the region from 900°C to below the silicon melting. In the end of the annealing process, a sharp and smooth interface is formed without polycrystalline silicon between the top silicon layer 312 and the buried oxynitride layer 331. The formed buried oxynitride layer 331 is a uniform amorphous layer free of bubbles. Because of the enhanced diffusion of various atoms in the amorphous region, the nitrogen atom, staying in the top silicon layer, rapidly migrates to buried oxynitride layer in the annealing process. The top silicon layer returns to single crystal silicon in the recrystallization process.

B4

- -

IN THE CLAIMS:

Please delete claims 19 and 20 without prejudice.

Please amend claims 1, 3 and 21-28 as follows:

1. (Amended) A method for fabricating a silicon-on-insulator (SOI) material on a silicon containing substrate having a major surface, comprising the steps of:

(1) implanting first kind of ions at a first dose and a first energy through said major surface into said silicon containing substrate controlled at a first temperature;

(2) implanting second kind of ions at a second dose and a second energy through said major surface into said silicon containing substrate at a second temperature below 100°C, to form an amorphous region beneath the major surface and to keep the original structure in the major surface of said silicon containing substrate; and

B5

(3) annealing aforesaid silicon containing substrate at a third temperature in the range from 1250°C to below the melting point of silicon, to form a buried layer by combining the first implanted ions in step (1) with silicon in the substrate, and a top silicon layer including the said major surface isolated by the buried layer, wherein the amorphous region contains a majority of a top silicon layer and the whole buried layer formed in step (3).

does not further limit

SUBC 17 B6

3. (Amended) The method of claim 1 wherein the third temperature is selected in the range from 900°C to 1250°C, eliminating the threading dislocations in the top silicon layer, and silicon islands and pinholes in buried oxide layer to form SOI material.

21. (Amended) The method of claim 3 wherein the first dose is in the range from 1×10^{16} cm^{-2} to 5×10^{18} cm^{-2}.

22. (Amended) The method of claim 3 wherein the first energy is chosen to form enough depth of said buried nitride layer after said annealing process in step (3), so as to form a desired thickness of the top silicon layer.

23. (Amended) The method of claim 22 wherein the first energy is in the range from 50keV to 400keV.

B7

24. (Amended) The method of claim 3 wherein the first temperature is chosen to keep the original structure in vicinity of said major surface on silicon containing substrate in said first implantation process of step (1).

25. (Amended) The method of claim 3 wherein the first temperature is in the range from 450°C to 700°C.

26. (Amended) The method of claim 3 wherein the second energy is chosen in the range from 30keV to 5MeV to form an amorphous region beneath the major surface and to keep the original structure in the major surface of said silicon containing substrate during the implantation in step(2).

Sub D7

27. (Amended) The method of claim 2 wherein the second dose is chosen in the range from 1×10^{13} cm^{-2} to 5×10^{16} cm^{-2} to form an amorphous region beneath the major surface containing both a majority of top silicon layer and all the buried oxide layer, which is formed in step(3).

28. (Amended) The method of claim 3 wherein the second kind of ion is silicon ion.

EXPLANATION OF AMENDMENT:

The specification has been amended as shown by [deletions] and insertions.

Paragraphs from page 6, line 32 through page 7, line 8:

(2) implanting second kind of ion at a second dose and a second energy though said major surface into said silicon containing substrate at a second temperature below 100°C to form an amorphous region beneath said major surface containing both a [in] majority of top silicon layer and the whole buried layer which is formed in step (3), and retain an original structure in said major surface of the silicon containing substrate, and to enhance the diffusion of atoms in the amorphous region; and

(3) annealing the silicon containing substrate at a third temperature in the range from [900] 1250°C to below the melting point of silicon, to combine the first implanted nitrogen and silicon to form a buried nitride layer and the top silicon layer, including the major surface isolated by the buried nitride layer.

Paragraphs from page 8, line 30 through page 9, line 30:

Figs.1A-1C show a schematic view of a cross-section of a SIMOX substrate at the stages of oxygen implantation, amorphous process and high temperature annealing for illustrating the elimination of threading dislocation in the formed SOI film.

Figs. 2A-2B show a schematic view of a cross-section illustrating the elimination of silicon islands and pinholes in the buried oxide layer in the already formed SOI substrate.

Figs. 3A-3C show a schematic view of a cross-section of a SIMNI substrate at the stages of nitrogen implantation, amorphous process and high temperature annealing for illustrating the formation of buried amorphous nitride layer in the formed SOI film.

Fig. [1] 4 shows an illustration of the random spectrum of Rutherford Backscattering Spectroscopy (RBS) of a SOI material fabricated by conventional method the routine

process. It can be seen that the thickness of the formed top silicon layer is about 200 nm and the thickness of the buried oxide layer is about 300 nm.

Fig. [2] 5 shows an illustration of an RBS channeling aligned spectrum of the sample, on which amorphous process is performed by a silicon self implantation. It can be seen that the amorphous region in the depth within 50nm to 500nm beneath the surface.

Fig. [3] 6 is a cross-sectional transmission electron micrograph (XTEM)of the sample, on which amorphous process is performed by a silicon implantation after an implantation of oxygen ion with dose of 1.6×10^{18} cm^{-2} and energy of 170keV into p-type (100) Si wafer, and then performed by rapid thermal annealing at temperature of 1150°C for 5 seconds. It can be seen that SOI three-layer structure has been formed primarily. The top silicon layer has been recrystallizing. There are no silicon islands in the buried layer.

Fig. [4] 7 is a cross-sectional transmission electron micrograph of a sample treated as in Fig. [3] 6 except for 5 seconds of rapid thermal annealing at temperature of 1250°C. It can be seen that the SOI three-layer structure with clear interface has been formed. Si islands have appeared in the buried layer.

Fig. [5] 8 is a cross-sectional transmission electron micrograph of the sample, on which amorphous process is performed by a silicon implantation after an implantation of oxygen ion with dose of 1.6×10^{18} cm^{-2} and energy of 180keV into p-type (100) Si wafer and subsequent annealing at temperature of 1300°C for 6 hours. It can be seen that there are silicon islands, but no threading dislocations in the SOI material.

Fig. [6] 9 is a cross-sectional transmission electron micrograph of a sample treated as in Fig. [5] 8 except for annealing at a lower temperature in the region from 900°C to 1250°C. It can be seen that there are no threading dislocations or silicon islands in the SOI material.

Fig. [7] 10 is a cross-sectional transmission electron micrograph of a sample, which is already an SIO substrate, [formed as in Fig. 5 and then silicon self-implantation is performed for forming amorphous region and subsequently] annealed at a temperature in

the range from 900°C to 1250°C. It can be seen also that there are no threading dislocations or silicon islands in the SOI material.

Paragraphs from page 10, line 3 through page 13, line 23:

As shown in Fig. 1A, based [Based] on amorphous process the improved SIMOX method is realized to form SOI material as follows:

At first, the silicon wafer 11 mounted to a holder as a target is heated to a temperature in the range from 450°C to 700°C, preferably about 500°C. It is heated usually by a set of halogen lamps in an implant chamber. The temperature of the target is kept constant by the electronic device during implantation. The wafer may be p-type (100) silicon or n-type silicon, or with other orientation as desired. Oxygen ions 01 are implanted into silicon substrate 11 through the polished surface[,] or [said] major surface 10. The dose of implanting oxygen ion is usually in the region from 1×10^{16} cm^{-2} to 5×10^{18} cm^{-2}. Conventionally, the dose in the region from 1.2×10^{18} cm^{-2} to 1.8×10^{18} cm^{-2} is chosen to form buried oxide layer 21 of thickness in the region from about 300 nm to about 400 nm. In the present invention, a lower dose may be chosen to form a thinner buried oxide layer. For example, a dose of 0.5×10^{18} cm^{-2} may correspond to the thickness of about 100 nm. The implantation energy is usually chosen in the region from 30keV to 400keV, depending on both the thickness of the top silicon layer 12 and the thickness of the formed buried oxide layer 21. Conventionally, the implantation energy is chosen in the region from 150keV to 180keV for forming a thickness of about 200 nm of the top silicon layer 12 and a desired thickness of buried oxide layer 21. In many cases, a silicon dioxide film with thickness from 0 to 100 nm is deposed on the polished surface 10 of silicon wafer before ion implantation. On one hand, it can prevent silicon wafer from the direct contamination of metal grain during ion implantation process. On the other hand, it can protect the smooth silicon surface when the silicon dioxide film is removed after ion implantation process. However, the silicon dioxide film should not to be too thick, because reduction of the

thickness of the top silicon layer is the cost for this process. For example, a suitable thickness of the silicon dioxide film is about 50 nm.

Following is the second ion implantation process for performing the amorphous process as shown in Fig. 1B. It is performed after reducing the temperature of target or in another implanter. The temperature of target 11 is usually selected to be lower than 100°C in this process, because the lower the target temperature, the wider the amorphous region at the same implantation dose. It is convenient if the target temperature is selected as about room temperature, more preferably at liquid nitrogen temperature (about 77 K). For the amorphous process, the implanting ion 02 may be chosen to be silicon ion, germanium ion, inert gases ion or oxygen ion. The silicon ion is preferred. Because silicon ion implantation is the self-implantation for a silicon wafer, it will not affect the quality of the silicon wafer if the irradiation damage is restored in the annealing process. The others, germanium ion can be used because it is the element in same group as silicon and has an infinite solid solubility in silicon. Inert gas ions can be used because the do not react with any other element, so they do not affect the quality of the silicon wafer when used in a small dose. Oxygen ion can be used because it is the same ion as that in the first implantation step and plays the same role in the subsequent annealing process.

After the selection of the implanting ions, the width of the amorphous region 201 will be mainly determined by the dose of implanting ion and the temperature of the wafer. In order to get high amorphous efficiency, the wafer temperature is confined below 100°C. Because the high temperature of the target will cause the sample annealing to restore the irradiation damage, that will reduce the amorphous region 201. The second implantation energy mainly determines the depth of the amorphous region. In this process, the implantation energy is chosen in the region from 30keV to 5MeV, the implantation dose is chosen in the region from 1×10^{13} cm^{-2} to 5×10^{16} cm^{-2}. In the conventional SIMOX method of thick buried oxide layer, silicon ion is selected as the second implanted ion, the implantation energy is chosen in the region from 100keV to 500keV and the dose is chosen in the region from 5×10^{13} cm^{-2} to 5×10^{15} cm^{-2}. The implantation energy and dose are so selected, that the amorphous layer 201 can contain both a majority of top silicon layer 12 and all the buried

oxide layer 21 under the condition of keeping the single crystal structure in the vicinity of major surface of silicon. According to Richmond's or Sigmund's theory, the implantation energy and dose may be calculated at first based on the decision of the thickness and the depth of the amorphous region, and then they may be validated by the RBS channeling effect.

The RBS spectra presented in Fig. [1] 4 and Fig. [2] 5 are used to analyze the results, which were acquired using an incident beam of 2.0MeV He^+ ions normal to the sample's surface and a detector positioned at an angle of 165° with incident beam. In both figures, the ordinate represents backscattering yield (counts) and the abscissa represents the channel number in the multi-channel analyzer. In the experimental condition, the depth of every channel is about 8.3 nm. Fig. [1] 4 shows the RBS random spectrum of a SOI sample made from a p-type (100) Si wafer after oxygen ion implantation and subsequent high-temperature annealing. The ion implantation was done at an energy of 180keV and a dose of $1.6\times10^{18}cm^{-2}$. The annealing as shown in Fig. 1C was conducted for 6 hours at 1300°C. It is shown in the [figure] Fig. 4 that the thickness of the top silicon layer is about 200nm and the thickness of the buried oxide layer 21 is about 300nm. As shown in the channeling aligned spectrum of Fig. [2] 5, the depth of amorphous region 201 is in the range from about 50nm to about 500nm. The peak in right side of the spectrum especially showing single crystal structure on the surface of the silicon wafer is clearly visible. The height of the peak increases because the channeling spectrum of the surface adjacent to heavy damaged region overlaps with that of amorphous region.

Subsequent is the third step, the annealing process as shown in Fig. 1C. In order to prevent the implanted oxygen from escaping out of the wafer and retain the smooth surface during high temperature annealing, a silicon dioxide film with thickness from just about 0 to about 500nm was deposed on the implanted sample at a temperature below 700°C. Preferably, a thickness of about 200nm to about 300nm is selected. Subsequent annealing is performed in an inert ambient nominally mixed with less than 2 percent of oxygen. The annealing temperature can be from about 1250°C to below the melting temperature of silicon, with the duration from about 1 to about10 hours.

The top silicon layer 12 rapidly recrystallizes starting from the major surface 10 because of the amorphous enhanced diffusion effect. In this recrystallization process a lot of interstitial silicon atoms in the top silicon layer 12 rapidly return to the lattice position of the silicon single crystal, which eliminates the causes for forming the threading dislocations, based on the amorphous enhanced diffusion effect. At the same time the silicon oxide grains in the top silicon layer 12 are dissolved, the dissolved oxygen atoms in the top silicon layer 12 rapidly migrate to the buried oxide layer 21, driven by chemical potential. This process restores the single crystal structure in the top silicon layer 12. All of these result in elimination or at least a significant reduction of threading dislocation and formation of a SOI material with a sharp and smooth interface. However, there can be silicon islands and pinhole in the buried oxide layer 21 as shown in Fig. [5] 8.

Referring now to the XTEM photographs in Fig. [3] 6 and Fig. [4] 7, it can be seen that an SOI three-layers structure has been formed primarily after a conventional oxygen ion implantation process and a subsequent amorphous process by silicon ion implantation. The top silicon layer 12 has been being recrystallized during the rapid thermal annealing at 1150°C for 5 seconds, and there do not emerge silicon islands in the buried layer 21. After the rapid thermal annealing at 1250°C for 5 seconds, the SOI three-layer structure has clear interfaces. Silicon islands do emerge in the buried layer 21, but there are no threading dislocations in the top silicon layer 12. It shows further that silicon islands in buried oxide layer 21 are the products of the segregation of silicon in high temperature annealing and that the threading dislocations do not emerge in top Si layer 12 of the amorphous process by silicon ion implantation 02. It may also be seen in Fig.3 and Fig.4 that a band of damage appears in silicon substrate subjacent the buried oxide layer. It is denominated as ion implantation end-of-range damage (EOR), which is caused by the insufficiency of annealing.

Fig. [5] 8 is an XTEM photograph of a sample made from p-type (100) silicon, which is formed by oxygen ion implantation at dose of 1.6×10^{18} cm^{-2} and energy of 180keV and subsequent silicon ion implantation for amorphizing the substrate in the range of depth from about 50nm to about 500nm. It was annealed finally at 1300°C for 6 hours.

Paragraphs at page 13, line 24 through page 15, line 29:

If the third step to perform annealing process goes on at a lower temperature selected from 900°C to 1250°C and the duration chosen from 1 second to 20 hours, a conventional annealing furnace can be used. Because of amorphous enhanced diffusion effect, atoms in the amorphous region various still have relatively high diffusion coefficient even at a lower annealing temperature. The process can suppress silicon segregation in the buried oxide layer at a low temperature, and accordingly form the SOI material without threading dislocations in BOX, and without silicon islands and pinholes in the buried layer as shown in the Fig. [6] 9.

Fig. [6] 9 is a XTEM photograph of a sample, which is formed in the same implantation condition and the same amorphous process as in Fig. [5] 8, but a low temperature annealing in the region from 900°C to 1250°C. It can be seen from the photograph that the SOI material is free of threading dislocations and silicon islands. There is a band of damage subjacent the buried oxide layer, which is the remaining end-of-range damage. Because of the isolation of the buried oxide layer such damage will not affect electrical properties of the devices made in the top silicon layer, but it may absorb the contaminating metal impurity produced the first implantation process.

As described and further illustrated by the present invention and figures, the silicon islands and pinholes 222 in the buried oxide layer 221 as shown in Fig. 2A are produced by silicon segregation in an over-high annealing temperature. In order to eliminate silicon islands in the formed SOI material, the present invention proposes following process: mounting the SOI wafer 211 to a holder, holding a temperature below 100°C, implanting silicon ion 02 through the top polished surface 210 into the SOI wafer at a dose in the region from 5×10^{13} cm^{-2} to 5×10^{15} cm^{-2} and a energy in the region from 100keV to 500keV. In this way, an amorphous region 2201 with the buried oxide layer 221 in it will be formed, but the top layer 212 in the vicinity of the front wafer surface 210 keeps its single crystal structure. And then it is annealed at a temperature above

900°C and below 1250°C in a conventional annealing furnace as shown in Fig. 2B and in an inert ambient atmosphere. There is no oxygen diffusing outwards, if only amorphous region does not extend to the top Si layer too much, which is shown by the XTEM photograph in Fig. [7] 10.

Fig. [7] 10 is a XTEM photograph of a sample, which is formed from the sample as in Fig. [5] 8 and then silicon self-implantation is performed for forming amorphous region and subsequently annealed at a temperature in the range from 900°C to 1250°C. It retains the single crystal structure in the top silicon layer and smooth interface, such as in Fig. [5] 8. However, it eliminates silicon islands in the buried layer. In the figure, there appear some damages beneath the lower interface of the buried oxide layer, which result from residual end-of-range damage.

In this sample, there are no threading dislocations in the top layer 212, nor silicon islands in the thicker buried oxide layer 221 prepared by SIMOX method. To the best knowledge of the inventor, such a remarkably good SOI sample is the first one.

In order to improve the separation technique by implantation of nitrogen and to solve the problems existing in the separation by implantation of nitrogen (SIMNI) and the separation by implantation of oxygen and nitrogen (SIMON), a similar set of steps are proposed for successfully forming high quality of SOI material fabricated by SIMNI or SIMON as shown in Figs. 3A-3C.

If a p-type (100) silicon substrate 311 of 500°C temperature is implanted by N^+ ion at 160keV energy and 1.0×10^{18} cm^{-2} dose, and subsequently annealed at high temperature as in the conventional process, the formed buried nitride layer 331 will be a polycrystal one. But if it is implanted subsequently by O^+ ion at 2×10^{17} cm^{-2} dose and aforesaid energy after the N^+ ion implantation, and then annealed at high temperature, the formed buried layer 331 will be an amorphous one. However, if this implanted oxygen dose is lower, there emerges a polycrystalline silicon in the top silicon layer 312 near amorphous buried oxynitride layer 331, which will disturb the formation of the sharp interface. If the dose of additional implanted oxygen is higher, nitrogen bubble will be formed insides the buried

layer 331. All of these are the reason for the low diffusion coefficient of nitrogen atom in the silicon nitride or silicon oxynitride layer.

In accordance with the present invention, after the implantation of N^+ ions or N^+, O^+ ions 03 an amorphous process will be carried out by silicon self-implantation at room temperature or liquid nitrogen temperature, with implantation energy in the region from 100keV to 500keV and dose in the region from 5×10^{13} cm^{-2} to 5×10^{15} cm^{-2}. In the precondition of keeping single crystal structure on silicon surface 310, an amorphous region 3201 will be formed beneath the surface 310, in which the buried oxynitride layer 331 will be formed. The implanted ions may be germanium ion, inert gas ions or oxygen ion as desired.

Subsequent is an annealing process at a temperature in the region from 900°C to below the silicon melting. In the end of the annealing process, a sharp and smooth interface is formed without polycrystalline silicon between the top silicon layer 312 and the buried oxynitride layer 331. The formed buried oxynitride layer 331 is a uniform amorphous layer free of bubbles. Because of the enhanced diffusion of various atoms in the amorphous region, the nitrogen atom, staying in the top silicon layer, rapidly migrates to buried oxynitride layer in the annealing process. The top silicon layer returns to single crystal silicon in the recrystallization process.

The claims have been amended as shown by [deletions] and insertions.

1. (Amended) A method for fabricating a silicon-on-insulator (SOI) material on a silicon containing substrate having a major surface, comprising the steps of:

(1) implanting first kind of ions at a first dose and a first energy through said major surface into said silicon containing substrate controlled at a first temperature;

(2) implanting second kind of ions at a second dose and a second energy through said major surface into said silicon containing substrate at a second temperature below 100°C, to form an amorphous region beneath the major surface and to keep the original structure in the major surface of said silicon containing substrate; and

(3) annealing aforesaid silicon containing substrate at a third temperature in the range from [900°] 1250°C to below the melting point of silicon, to form a buried layer by combining the first implanted ions in step (1) with silicon in the substrate, and a top silicon layer including the said major surface isolated by the buried layer, wherein the amorphous region contains a majority of a top silicon layer and the whole buried layer formed in step (3).

3. (Amended) The method of claim 1 wherein the [said] third temperature is selected in the range from 900°C to 1250°C, eliminating the threading dislocations in the top silicon layer, and silicon islands and pinholes in buried oxide layer to form SOI material.

21. (Amended) The method of claim 3 wherein the [said] first dose is in the range from 1×10^{16} cm^{-2} to 5×10^{18} cm^{-2}.

22. (Amended) The method of claim 3 wherein the [said] first energy is chosen to form enough depth of said buried nitride layer after said annealing process in step (3), so as to form a desired thickness of the top silicon layer.

23. (Amended) The method of claim 22 wherein the [said] first energy is in the range from 50keV to 400keV.

24. (Amended) The method of claim 3 wherein the [said] first temperature is chosen to keep the original structure in vicinity of said major surface on silicon containing substrate in said first implantation process of step (1).

25. (Amended) The method of claim 3 wherein the [said] first temperature is in the range from 450°C to 700°C.

26. (Amended) The method of claim 3 wherein the [said] second energy is chosen in the range from 30keV to 5MeV to form an amorphous region beneath the [said] major surface and to keep the original structure in the major surface of said silicon containing